REMARKS/ARGUMENTS

Favorable consideration of this application in light of the following discussion is respectfully requested.

Claims 1-4 are pending in this application.

In the outstanding Office Action, Claim1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee (U.S. Patent 5,426,447) in view of Masahiko (Japanese Patent Publication No. 63-261326); Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Masahiko as applied to Claim 1 above, and further in view of Kwon (U.S. Patent No. 5,850,216); Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Masahiko as applied to Claim 1 above, and further in view of Koyama et al. (U.S. Patent No. 6,177,920; hereinafter Koyama); and Claim 3 was indicated as containing allowable subject matter.

Briefly recapitulating, the present invention is directed to a process for displaying data on a matrix display having N data lines and P selection lines. At the intersections of these lines are image points or pixels in which the N data lines are grouped into P blocks of N' data lines (N = P x N'). Each block receives in parallel one of the P data signals which is demultiplexed on the N' lines of the block. The N' data lines of a block are alternately scanned from 1 to N' and from N' to 1 according to the selection lines. This allows for a display without introducing a DC error of several tens of mV between the first column sampled in the block and the last, as is common in conventional systems.[1]

As noted in the interview, Figure 1 shows an exemplary configuration of N data lines (vertical lines) divided into P blocks of N' lines (e.g., N'= 9 and lines C1-C9 comprise the first portion), and M sampling lines (e.g., horizontal lines L1 – L4). Each block receives in parallel one of the P data signals which are demultiplexed by sampling signals (DW1 –

[1] Specification, page 3, lines 11-21.

DW9), wherein the timing of the sampling signals is controlled so that for the claimed patterns of forward and backward scans are performed.[2]

Lee discloses a method for demultiplexing Y data selection signals over X groups of Y data lines. In particular, Lee discloses pixels located at the intersection of data lines and row lines.[3] In Lee, the number of data lines is equal to the number of groups multiplied by the number of data lines/group.[4] As noted in the Office Action,[5] Lee does not disclose alternately scanning of the N' data lines of a block from 1 to N' and from N' to 1 according to the selection lines as recited in Applicants' Claim 1.

Masahiko discloses a driving circuit for an electro-optic device where brightness differences for each line are averaged by alternately leading out column electrode lines on left and right [columns] and reversely setting the scanning order of select pulses supplied to the left column electrode line group and the scanning order of select pulses supplied to the right column electrode line group.[6] However, contrary to the Official Action, Masahiko, like Lee, does not disclose alternately scanning of the N' data lines of a block from 1 to N' and from N' to 1 according to the selection lines as recited in Applicants' Claim 1. In Masahiko, the columns are divided into a right column and a left column, where the right column is scanned in a first direction while the left column is scanned in an opposite direction. However, the scan directions are not reversed for alternate lines as recited in Applicants' Claim 1.

Applicants have also considered Kwon and Koyama and submit that neither of these references cure the deficiencies of Lee and Masahiko. Kwon teaches changing a scanning direction of a single line based on a scanning signal DWN.[7] Koyama teaches a synchronous

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[2] Specification, page 4, line 27 – page 5, line 16.
[3] Lee, column 5, lines 31-37 and column 6, lines 33-41.
[4] Lee, column 6, lines 48-60.
[5] Office Action, page 6, lines 3-4.
[6] Masahiko, page 8, lines 20-26.
[7] Kwon, column 10, lines 64-67.

clock signal to change a scanning direction of a single line.[8] Neither Kwon nor Koyama teach or suggest alternately scanning of the N' data lines of a block from 1 to N' and from N' to 1 according to the selection lines, as recited in Applicants' Claim 1.

Thus, as none of the cited prior art, individually or in combination, disclose or suggest all the elements of independent Claim 1, Applicants submit the inventions defined by Claim 1, and all claims depending therefrom, are not rendered obvious by the asserted prior art for at least the reasons stated above.[9]

Accordingly, in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully request an early and favorable action to that effect.

Respectfully submitted,

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[8] Koyama, column 8, lines 27-44.
[9] MPEP § 2142 "...the prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."